EE 435
Lecture 42

Over Sampled Data Converters
Output Stages in Op Amps

Final Exam:

Scheduled on Final Exam Schedule:

Wednesday May 5 9:45 a.m.

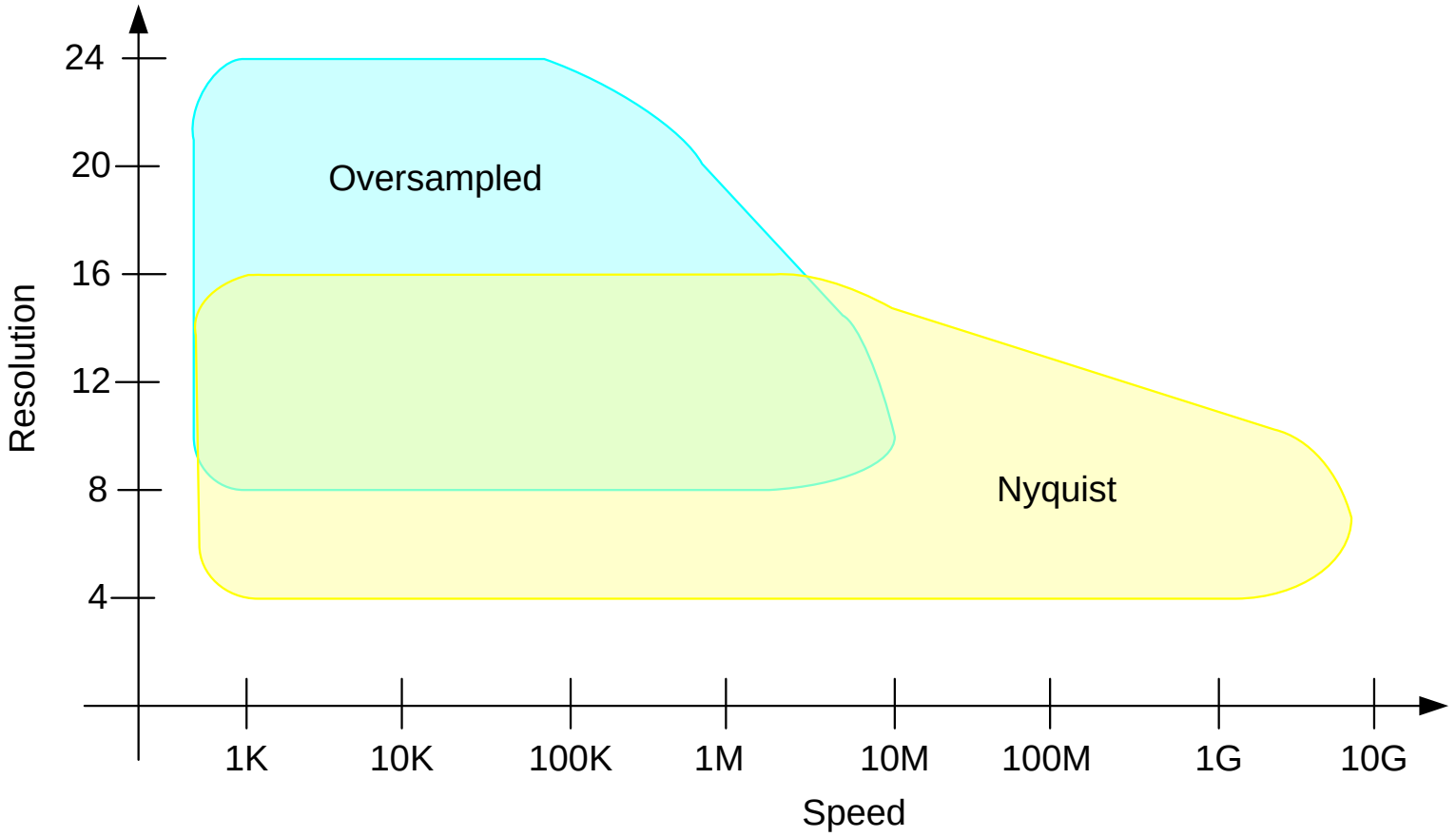
Revised Final Exam:

- Take-home format – open book and open notes
- Will be posted on course WEB site by late Friday April 30
- Due at 5:00 p.m. on Wednesday May 5 : Upload as pdf file into Canvas

If anyone has any constraints of any form such as internet access or other factors that makes it difficult to work with this revised format, please contact Professor Geiger by 5:00 p.m. on Wednesday April 28

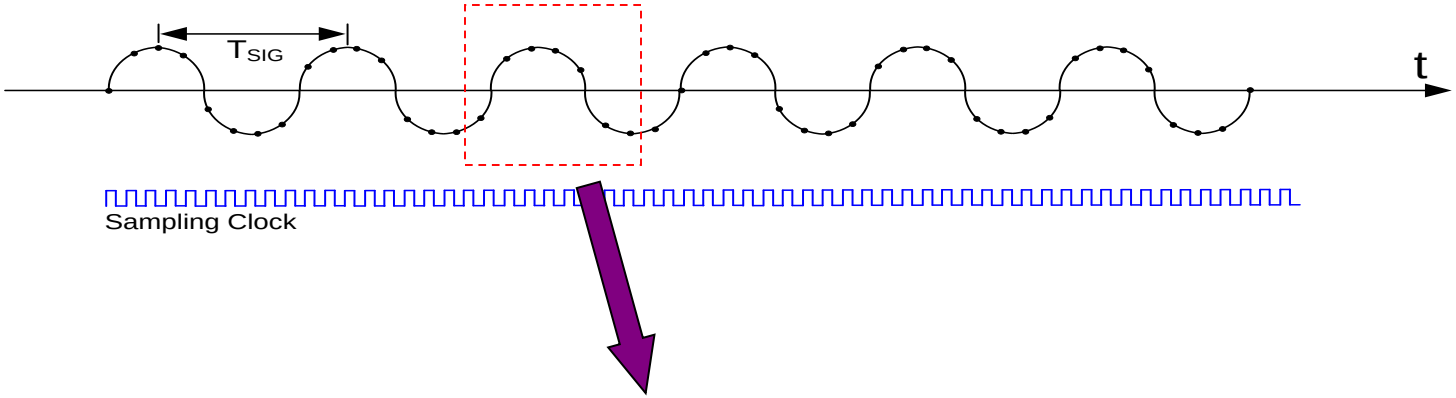
Review from Last Lecture

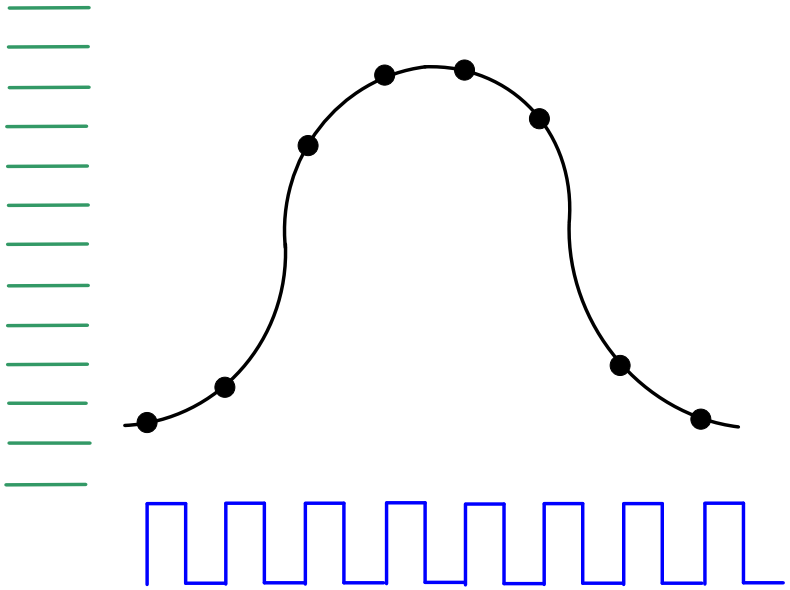
Data Converter Type Chart



Review from Last Lecture

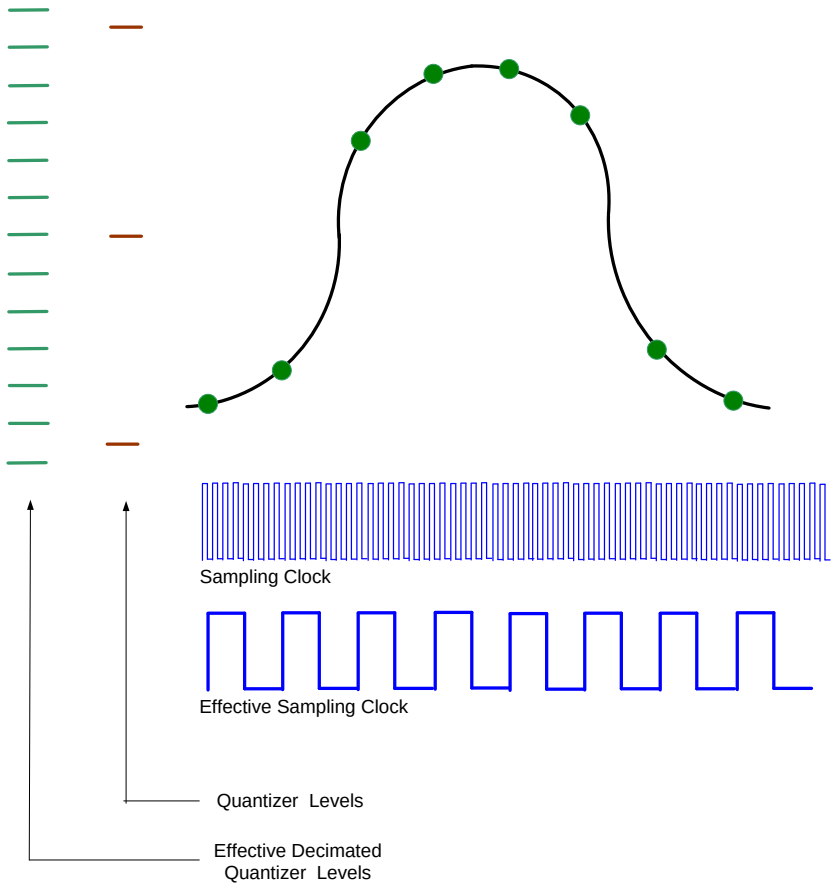
Nyquist Rate





Review from Last Lecture

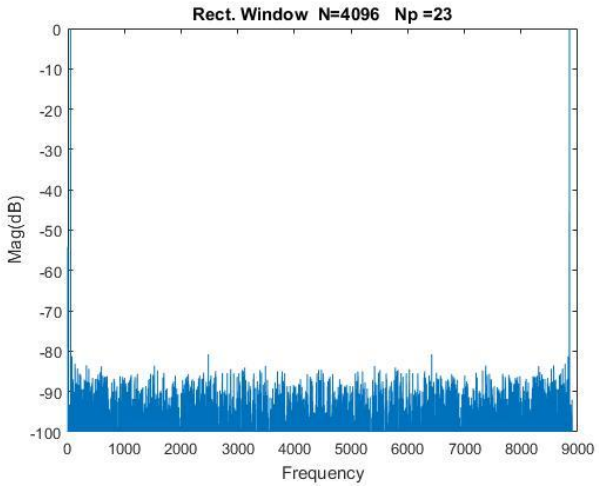
Over-Sampled



Over-sampling ratios of 128:1 or 64:1 are common
Dramatic reduction in quantization noise effects
Limited to relatively low frequencies

Review from Last Lecture

Over-Sampling



Res = 10 bits

f_{SIG}=50Hz
f_{NYQ}=100Hz
f_{SAMP}=8904KHz
Oversampled: 89:1

$$E_{RMS} = \frac{x_{LSB}}{\sqrt{12}}$$

What would happen if we break the 4096 samples into groups of 20 samples and form?

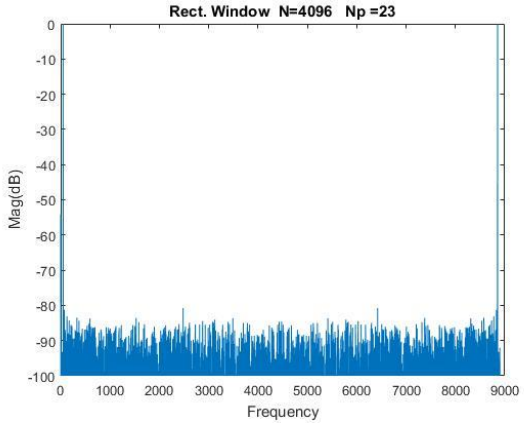
$$\hat{X}_{OUT}(k \bullet 20T_{SAMP}) = \frac{1}{20}\sum_{j=1}^{20} x_{OUT}\left(jT_{SAMP} + 20kT_{SAMP}\right)$$

$E_{RMS} = ?$

- Though the individual samples have been quantized to 10 bits, the arithmetic operations will have many more bits
- The effective sampling rate has been reduced by a factor of 20 but is still over 4 times the Nyquist rate
- Has the quantization noise been reduced (or equivalently has the resolution of the ADC been improved?
- Is there more information available about the signal?

Review from Last Lecture

Over-Sampling

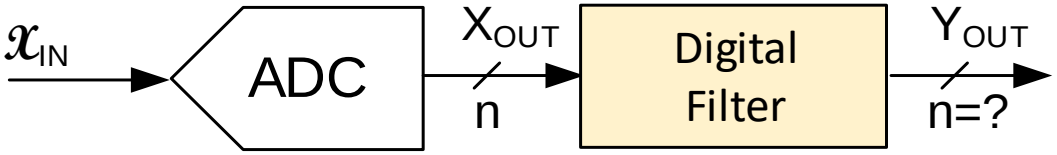


Res = 10 bits

f_{SIG}=50Hz
f_{NYQ}=100Hz
f_{SAMP}=8904KHz
Oversampled: 89:1

$$E_{RMS} = \frac{x_{LSB}}{\sqrt{12}}$$

Since the quantization noise is at high frequencies, what would happen if filtered the Boolean output signal?

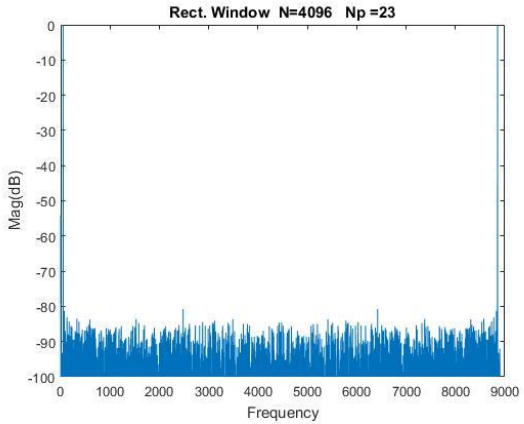


$$E_{RMS} = ?$$

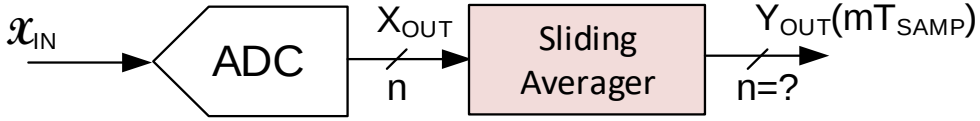
$$Y_{OUT}(kT_{SAMP}) = \sum_{j=0}^{m} a_j x_{OUT}(k - jT_{SAMP})$$

Or $$Y_{OUT}(kT_{SAMP}) = \sum_{j=0}^{m} a_j x_{OUT}(k - jT_{SAMP}) + \sum_{j=1}^{h} b_j Y_{OUT}(k - jT_{SAMP})$$

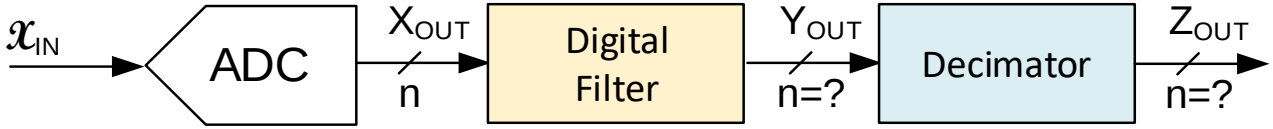
Over-Sampling



$$E_{RMS} = \frac{x_{LSB}}{\sqrt{12}}$$



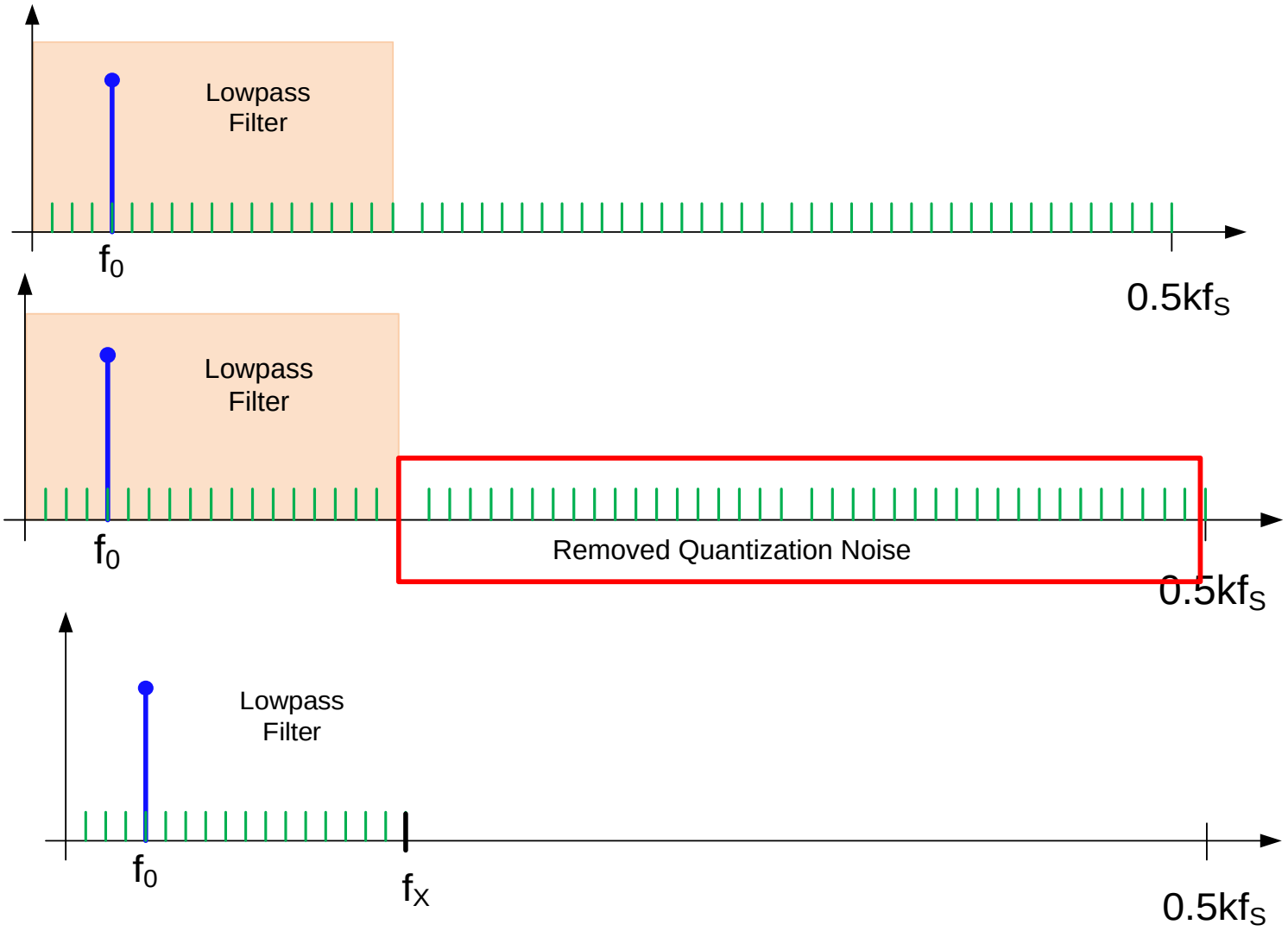
$$E_{RMS} = ?$$



$$E_{RMS} = ?$$

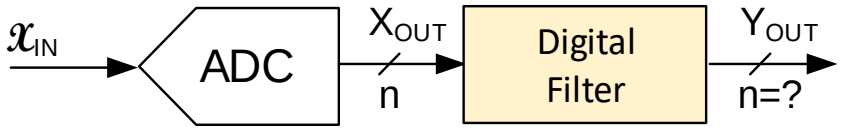
- What is the overhead?
- What is the performance potential?
- How can these or related over-sampling approaches be designed?
- Though this approach may help quantization noise, will not improve ADC linearity

Over-Sampled Spectrum showing quantization noise with digital lowpass filter



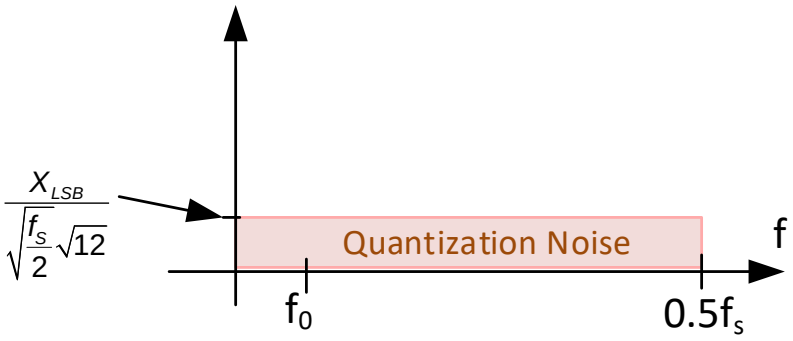
Residual Quantization Noise if Filter Band-edge at f_X

Over-Sampling



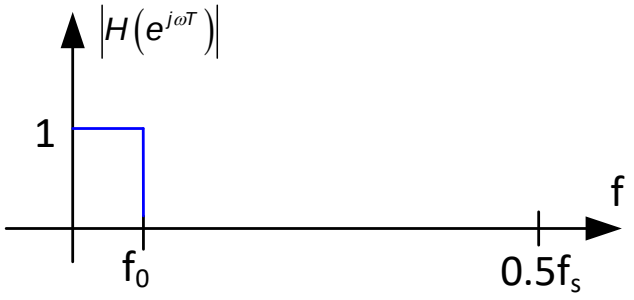
$f_S = f_{SAMP}$

$$OSR = \frac{f_S}{2}\frac{1}{f_0}$$



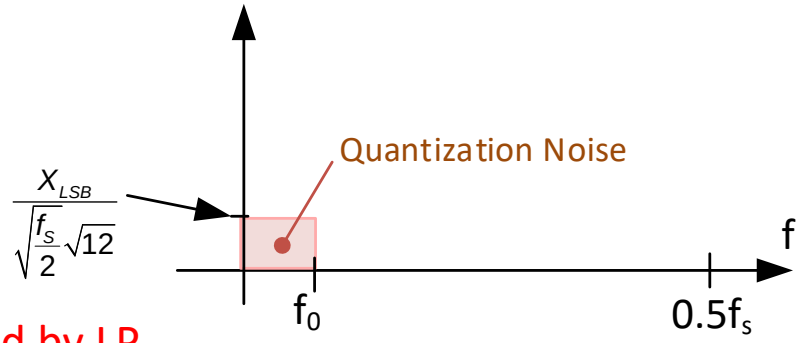
With ideal lowpass filter with band-edge at f_0

$$V_{Qrms} = \frac{V_{LSB}}{\sqrt{12}}\frac{1}{\sqrt{OSR}}$$



For sinusoidal input with p-p value V_{REF}

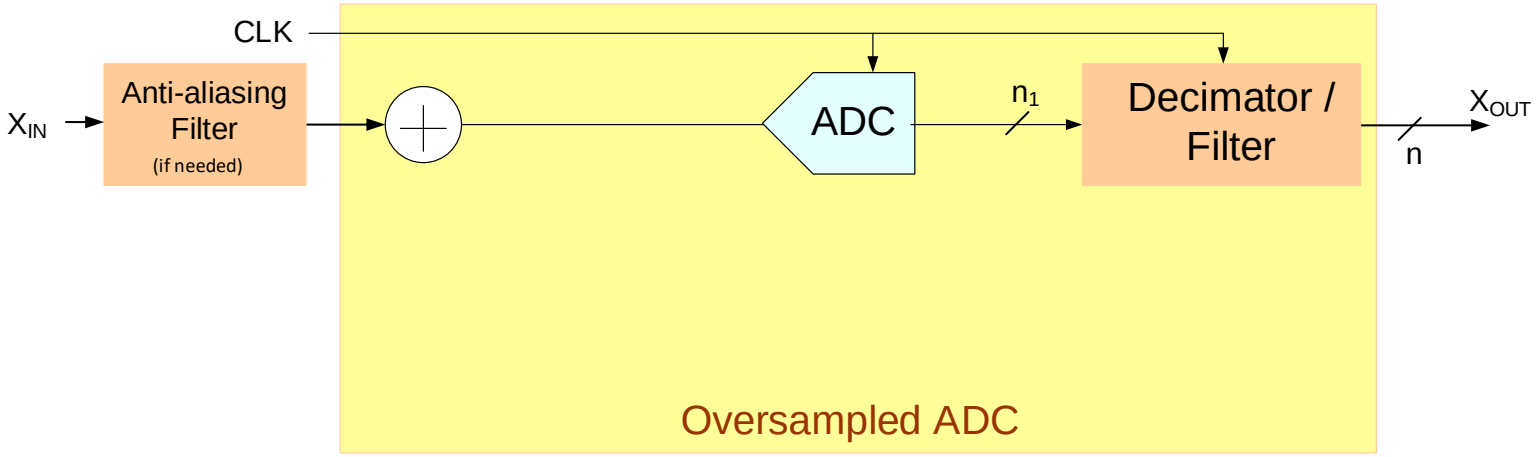
$$SNR = 6.02n + 1.76 + 10\log(OSR)$$



Improvement of 3dB/octave or 0.5bits/octave

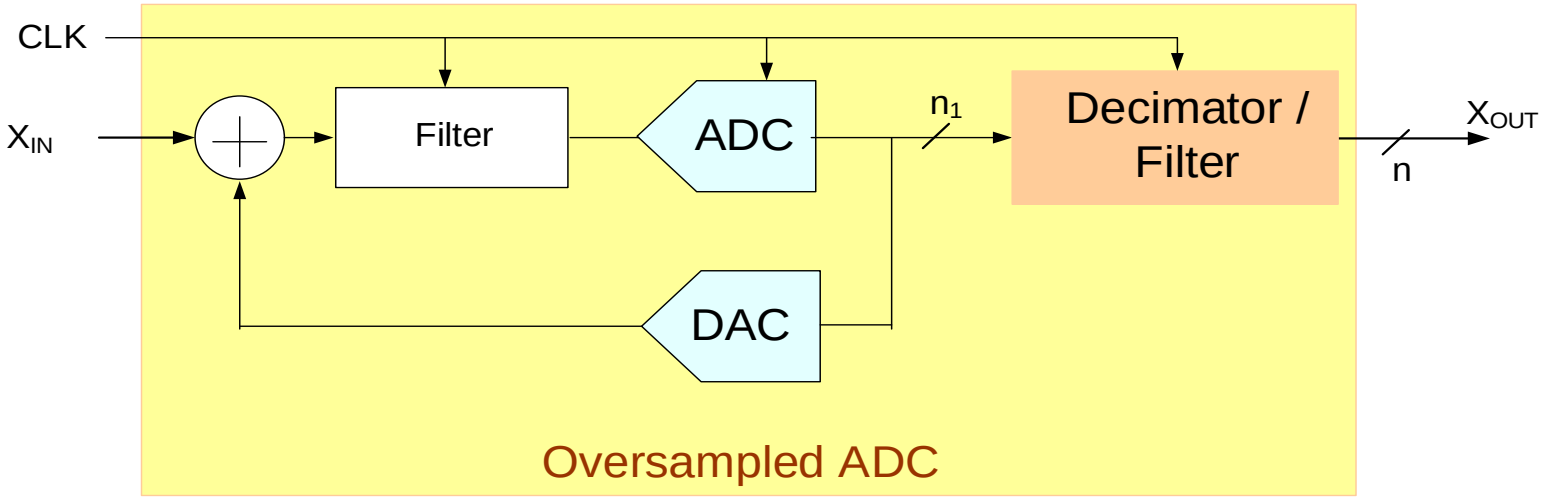
Oversampling increases resolution and if followed by LP filter Reduces Quantization Noise!

Over-sampled ADC



- Anti-aliasing filter at the input (if needed) to limit bandwidth of input signal
- ADC is often simply a comparator
- CLK is much higher in frequency than effective sampling rate (maybe 128:1 though lower OSR also widely used)
- Can obtain very high resolution but effective sampling rate is small
- **With clever design, this approach can reduce quantization effects and improve linearity**

Over-sampled ΔΣ ADC (Delta-Sigma)



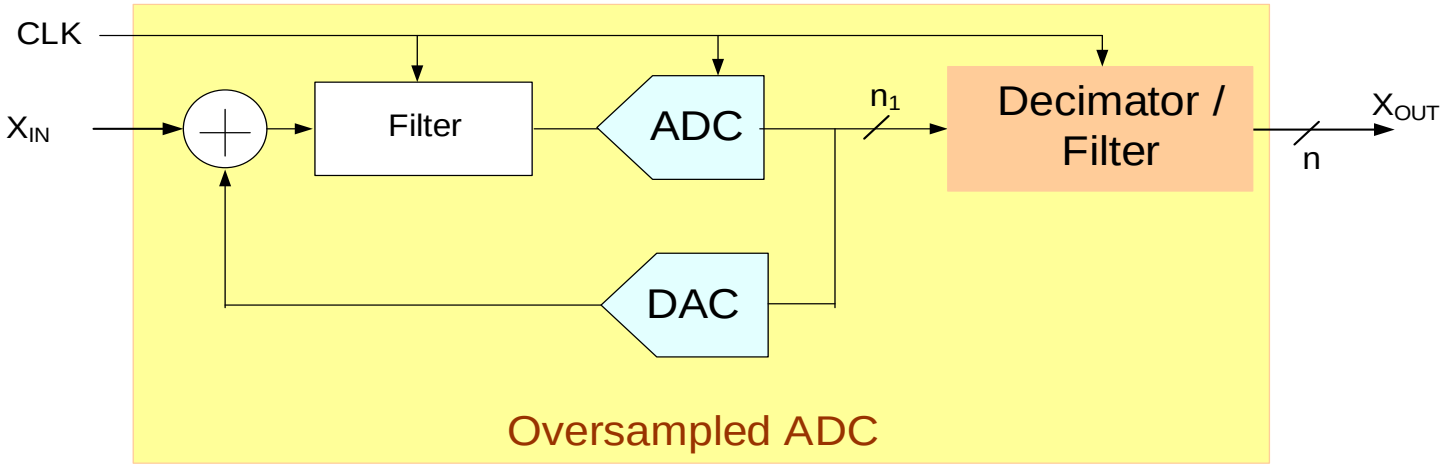
If Modulator is added, the over-sampled ADC becomes a ΔΣ ADC

Δ modulation introduced by Deloraine in 1946

ΔΣ ADC concept introduced by Yasuhiko Yasuda in the early 1960's while he was a student at the University of Tokyo

Candy (1974) and Temes credited with incorporating the concept in integrated data converters

Over-sampled ΔΣ ADC (Delta-Sigma)

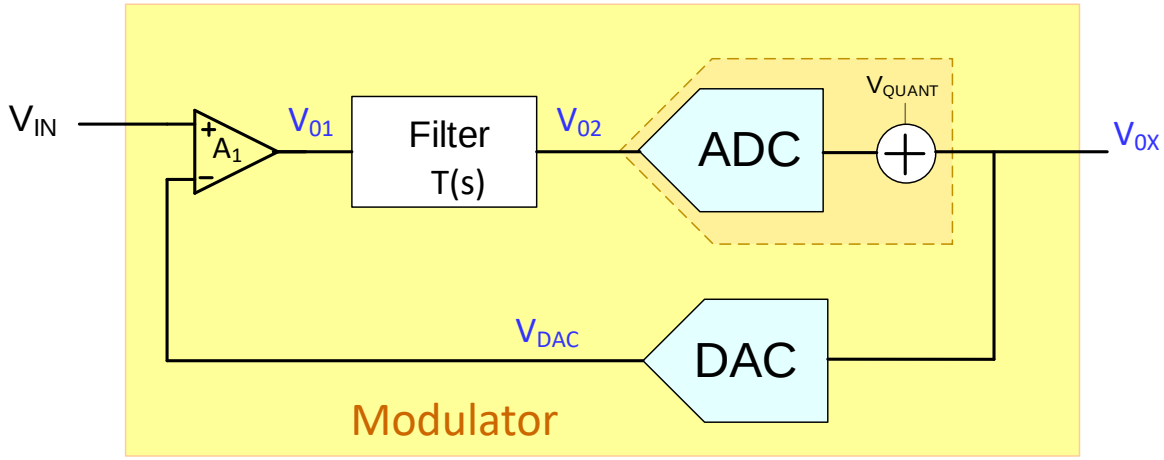


- Linearity performance almost entirely determined by that of the DAC
- 1-bit DAC (i.e. only a comparator for ADC) is inherently linear and widely used
- 20-bit linearity is achievable without any trimming using 1-bit DAC

Example: To obtain 16-bit linearity with a 10-bit DAC, the 10-bit DAC must be linear to at least the 16-bit level. This would usually require tedious trimming of the DAC

Analysis of Delta-Sigma ADC

(big benefit is noise shaping)



$$V_{01} = A_1\left(V_{IN} - V_{DAC}\right)$$

$$V_{02} = T(s)\,V_{01}$$

$$V_{OX} = V_{O2} + V_{QUANT}$$

$$V_{DAC} = V_{OX}$$

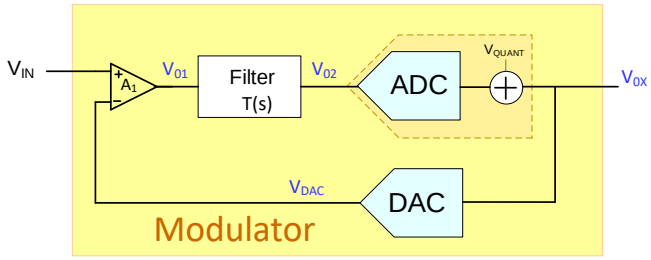
Solving, we obtain

$$V_{OX} = \frac{T(s)A_1}{1+T(s)A_1}V_{IN} + V_{QUANT}\frac{1}{1+T(s)A_1}$$

Note: Significantly different transfer functions for V_{IN} and V_{QUANT}

Analysis of Delta-Sigma ADC

(big benefit is noise shaping)



$$V_{OX} = \frac{T(s)A_1}{1+T(s)A_1}V_{IN} + V_{QUANT}\frac{1}{1+T(s)A_1}$$

Consider using an integrator for T(s)

$$T(s) = \frac{I_{01}}{s}$$

I_{01} is the unity gain frequency of the integrator and is a critical parameter in the modulator

Thus

$$V_{OX} = \frac{I_{01}A_1}{s+I_{01}A_1}V_{IN} + V_{QUANT}\frac{s}{s+I_{01}A_1}$$

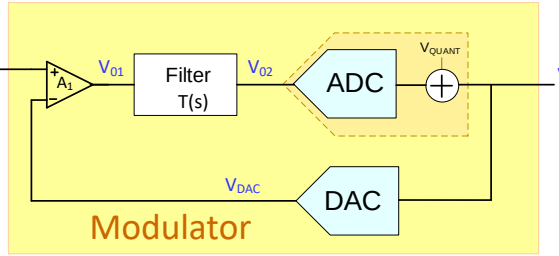
Note V_{IN} is low-pass filtered and V_{QUANT} is high-pass filtered and both are first-order with the same poles

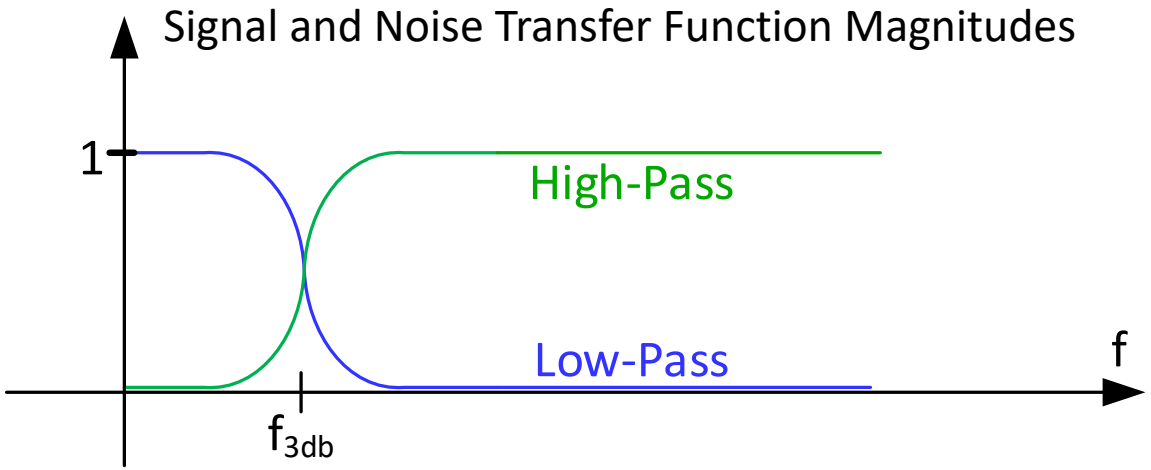
Analysis of Delta-Sigma ADC

(big benefit is noise shaping)

$$V_{OX} = \frac{I_{01}A_1}{s + I_{01}A_1} V_{IN} + V_{QUANT} \frac{s}{s + I_{01}A_1}$$

With integrator for T(s)



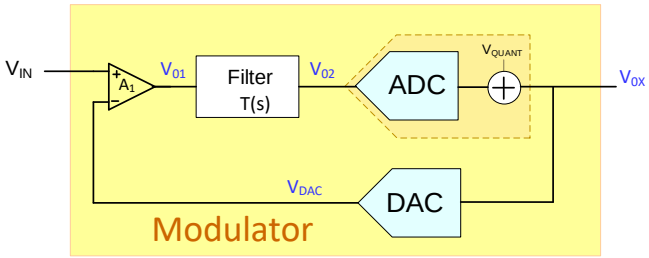


- Noise filtering will remove most of the noise from the signal band if the pole placed around signal band edge
- Signal band will not be significantly affected
- Filtering the noise is termed “noise shaping” in the vernacular of the delta-sigma community
- Since gain is 1 at high frequencies, HP filter does not increase spectral magnitude of noise at high frequencies

Analysis of Delta-Sigma ADC

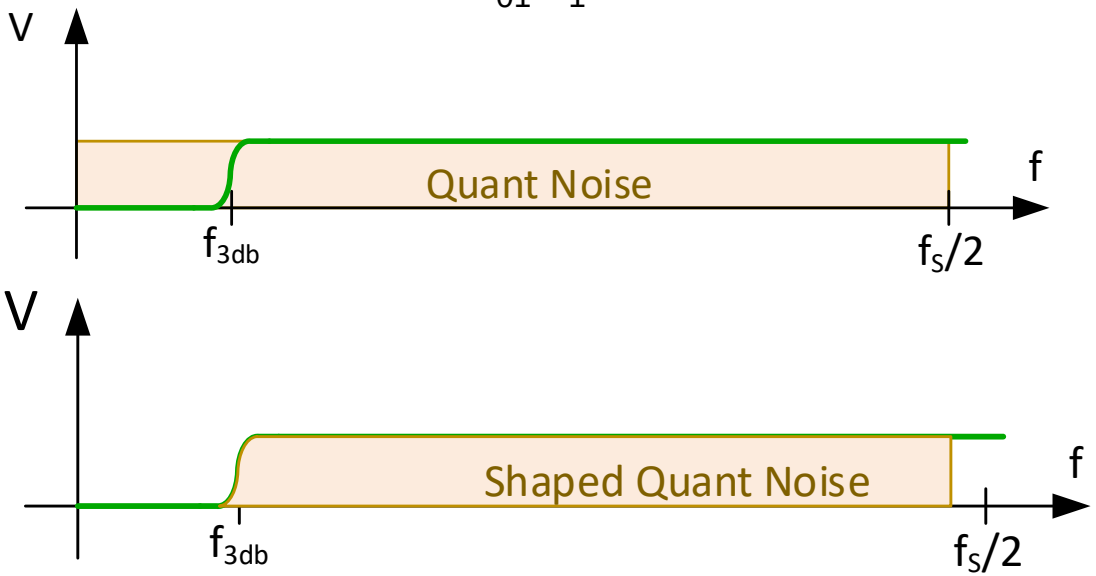
(big benefit is noise shaping)

$$V_{OX} = \frac{I_{01}A_1}{s + I_{01}A_1} V_{IN} + V_{QUANT} \frac{s}{s + I_{01}A_1}$$



Consider the noise output first

$$V_{OX-noise} = V_{QUANT} \frac{s}{s + I_{01}A_1} \qquad f_{3dB} = I_{01}A_1$$

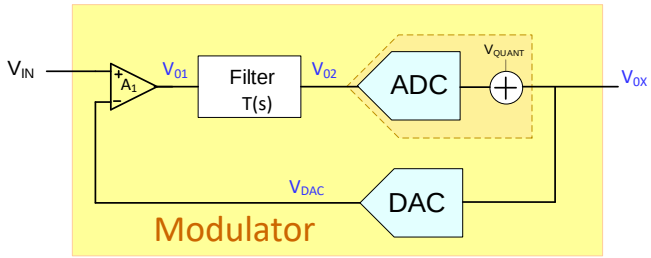


Major change in quantization noise spectral density at output

Analysis of Delta-Sigma ADC

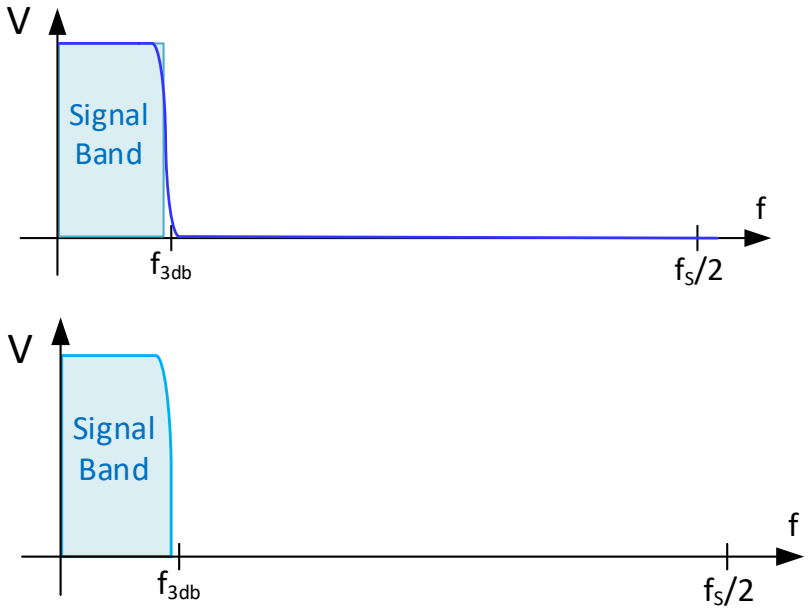
(big benefit is noise shaping)

$$V_{OX} = \frac{I_{01}A_1}{s + I_{01}A_1} V_{IN} + V_{QUANT} \frac{s}{s + I_{01}A_1}$$



Consider the input signal

$$V_{OX-IN} = V_{IN} \frac{I_{01}A_1}{s + I_{01}A_1} \qquad f_{3dB} = I_{01}A_1$$

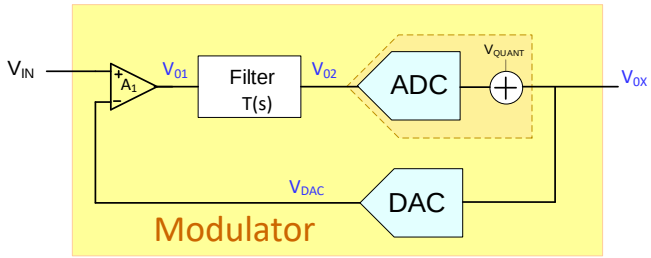


Little change in spectrum of input at the output

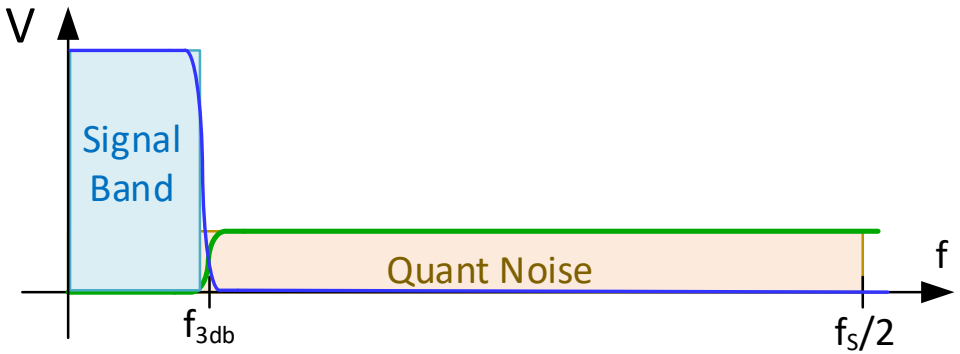
Analysis of Delta-Sigma ADC

(big benefit is noise shaping)

$$V_{OX} = \frac{I_{01}A_1}{s + I_{01}A_1} V_{IN} + V_{QUANT} \frac{s}{s + I_{01}A_1}$$



Combined effects



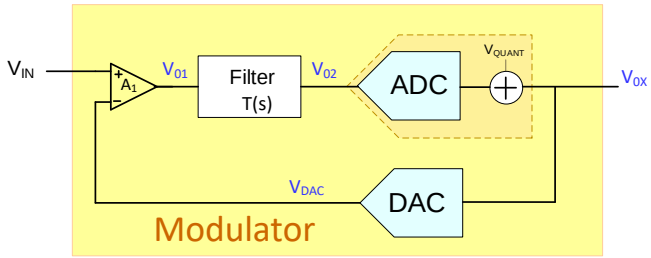
Remaining quantization noise can be dramatically reduced by a low-pass digital filter following modulator with band-edge around f_{3dB}

The low-pass digital filter would have little effect on the signal band

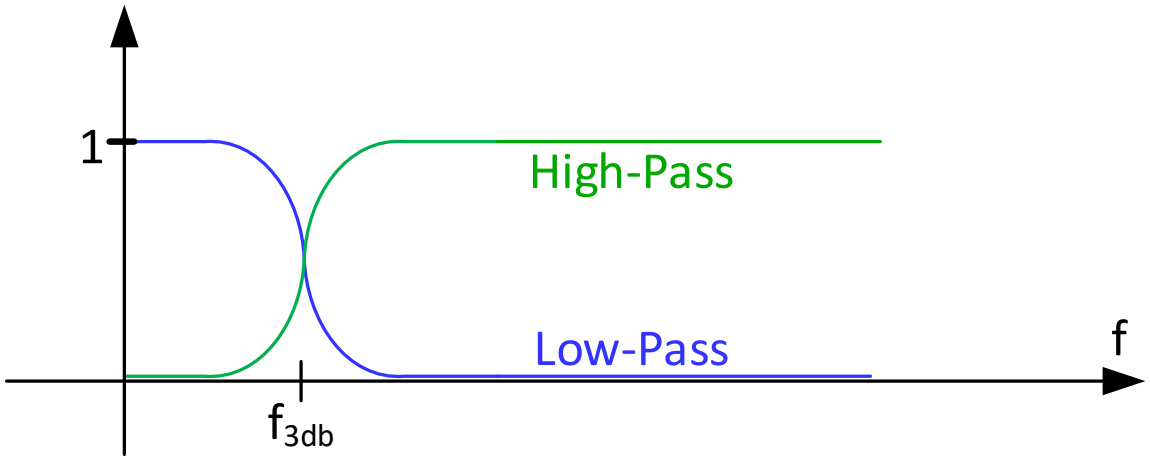
Analysis of Delta-Sigma ADC

(big benefit is noise shaping)

$$V_{OX} = \frac{T(s)A_1}{1+T(s)A_1}V_{IN} + V_{QUANT}\frac{1}{1+T(s)A_1}$$



Signal and Noise Transfer Function Magnitudes

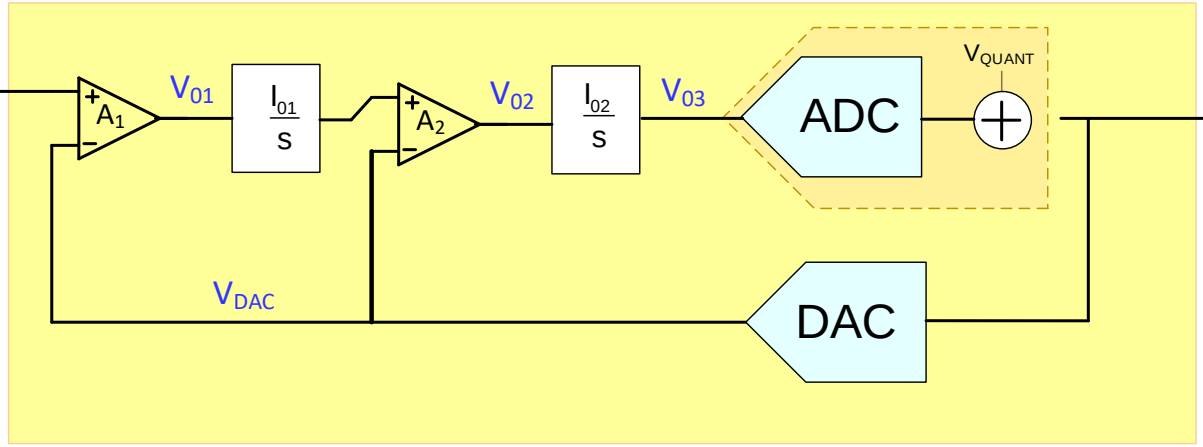


- A more selective filter (of higher order) would shape the noise even more and affect the passband even less if band edges are coincident

- Ideal low-pass and high-pass filters with coincident band edges followed by digital filter at output would allow nearly complete removal of the quantization noise !!

Second-order Delta-Sigma ADC

(big benefit is noise shaping)



Modulator only shown with two integrators

$$V_{01} = A_1\left(V_{IN} - V_{DAC}\right)$$

$$V_{02} = A_2\left[\frac{I_{01}}{s}V_{01} - V_{DAC}\right]$$

$$V_{03} = \frac{I_{02}}{s}V_{02}$$

$$V_{OX} = V_{O3} + V_{QUANT}$$

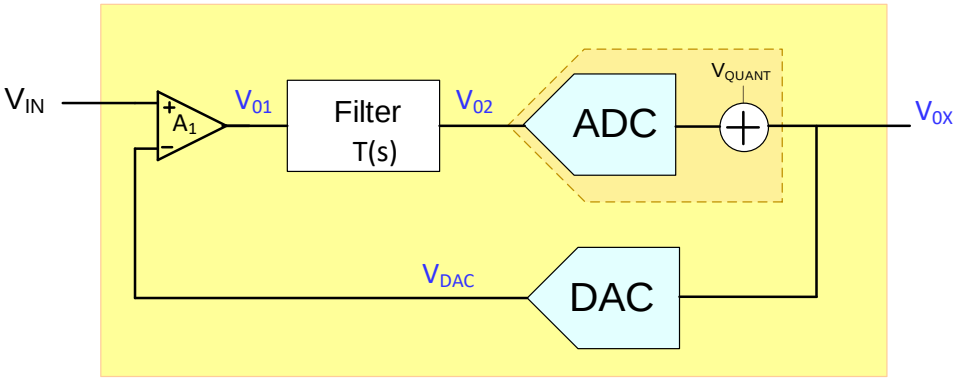
$$V_{DAC} = V_{OX}$$

Solving, obtain

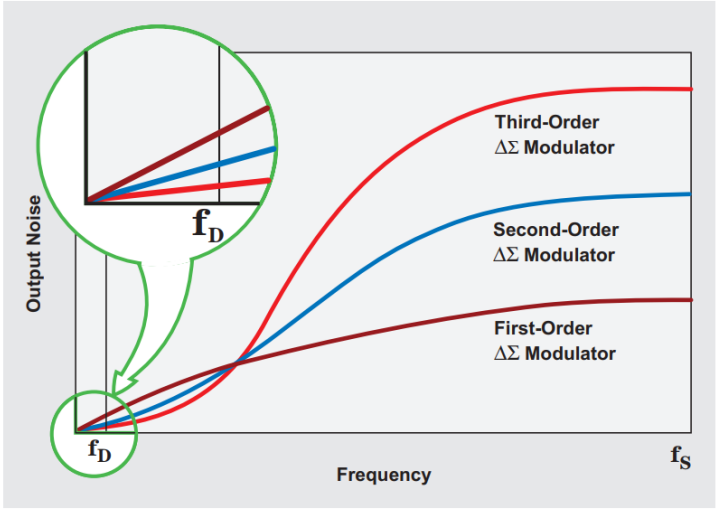
$$V_{OX} = \frac{I_{01}I_{02}A_1A_2}{s^2 + sI_{02}A_2 + I_{01}I_{02}A_1A_2}V_{IN} + \frac{s^2}{s^2 + sI_{02}A_2 + I_{01}I_{02}A_1A_2}V_{QUANT}$$

Higher-order Delta-Sigma ADC

(big benefit is noise shaping)



Much sharper transition between noise pass-band and signal stop band



From SLYT423 by Texas Instruments (author Bonnie Baker)

Baker reported TI used up to 6th order filters in SLYT423

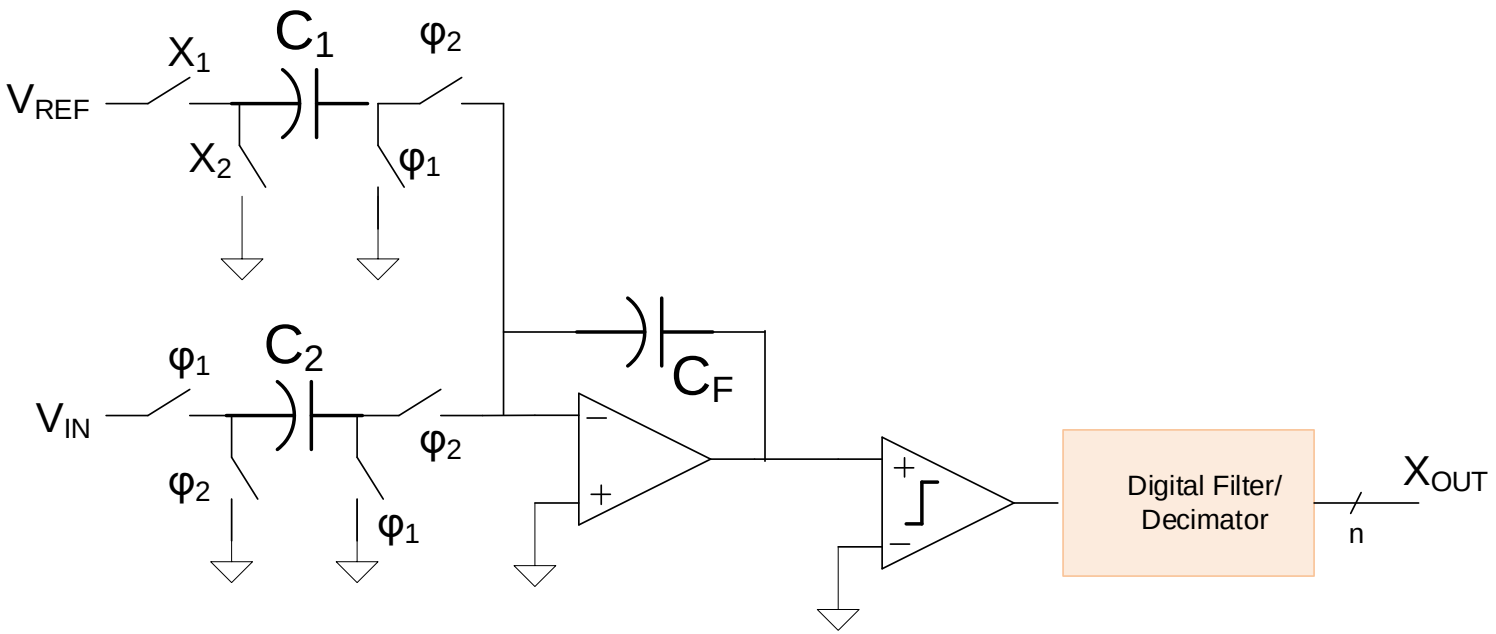
First-Order Delta-Sigma ADC

IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—I: FUNDAMENTAL THEORY AND APPLICATIONS, VOL. 50, NO. 3, M

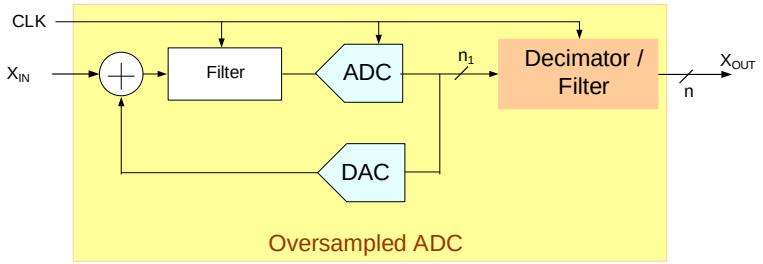
Behavioral Modeling of Switched-Capacitor Sigma–Delta Modulators

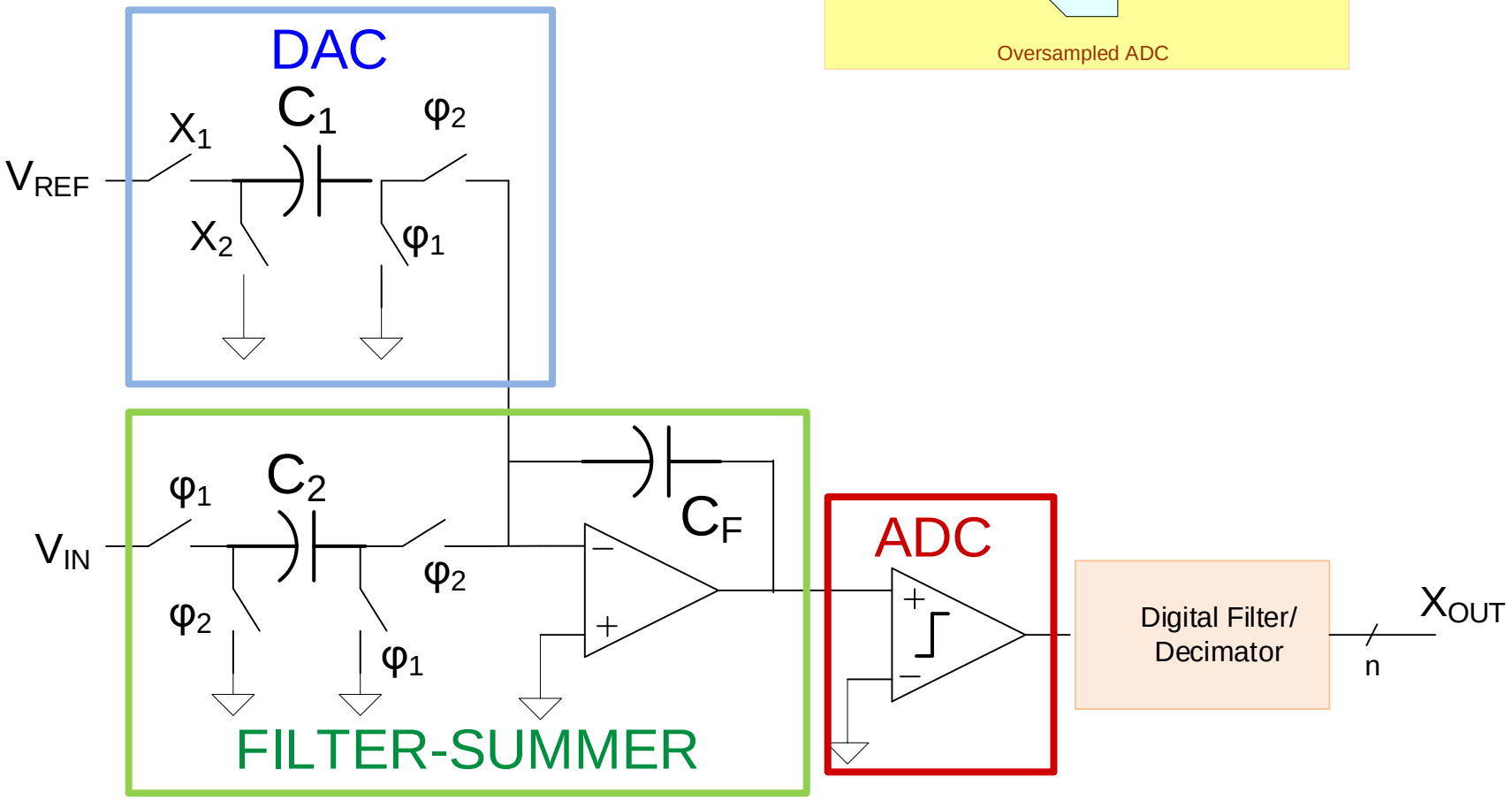
Piero Malcovati, *Member, IEEE*, Simona Brigati, *Member, IEEE*, Fabrizio Francesconi, *Member, IEE*
Franco Maloberti, *Fellow, IEEE*, Paolo Cusinato, and Andrea Baschirotto, *Senior Member, IEEE*

SC Circuits often used for Modulator



First-Order Delta-Sigma ADC





Over-sampled ΔΣ ADC)

Oversampling Alone:

$$SNR = 6.02n + 1.76 + 10\log(OSR)$$

0.5 bits/octave

Oversampling and First-Order Modulator:

$$SNR = 6.02n + 1.76 - 5.17 + 30\log(OSR)$$

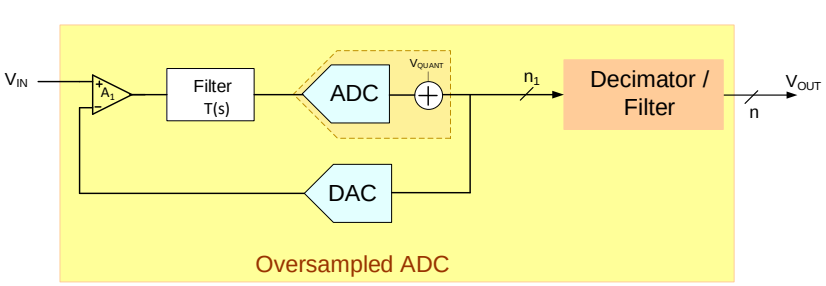
1.5 bits/octave

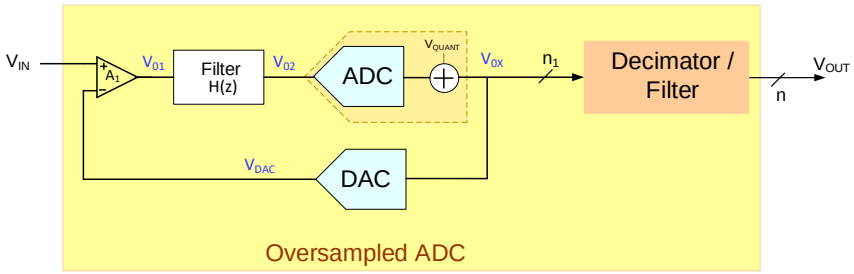
Oversampling and Second-Order Modulator:

$$SNR = 6.02n + 1.76 - 12.9 + 50\log(OSR)$$

2.5 bits/octave

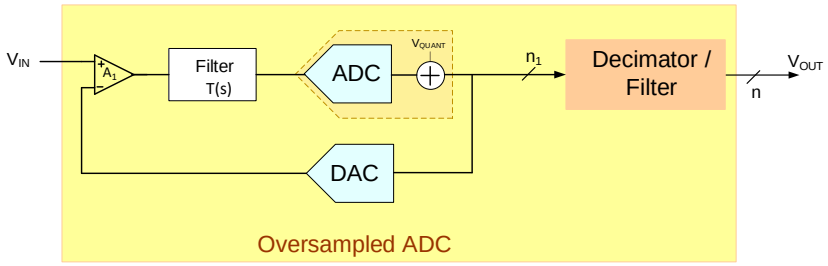
Continuous-Time vs Discrete-Time Over-sampled Delta-Sigma ADCs

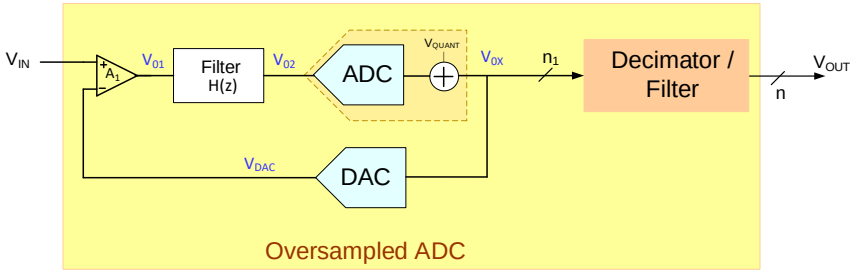




1. Input sampling errors for DT structures are never recovered
2. Nonlinearity of switches of concern in DT structures
3. No good switched in bipolar processes
4. Clock jitter adversely affects performance of discrete-time structures
5. Slew-rate requirements higher for DT structures and signal swings generally higher too
6. DT structures need additional headroom for switch control
7. CT structures can operate at lower supply voltages and lower power levels
8. Linearity of filter of increased concern in CT structures (particularly when using gm-C filters)
9. Transient response of DAC of increased concern in CT structures

Peculiar Issues with Over-sampled Delta-Sigma ADCs

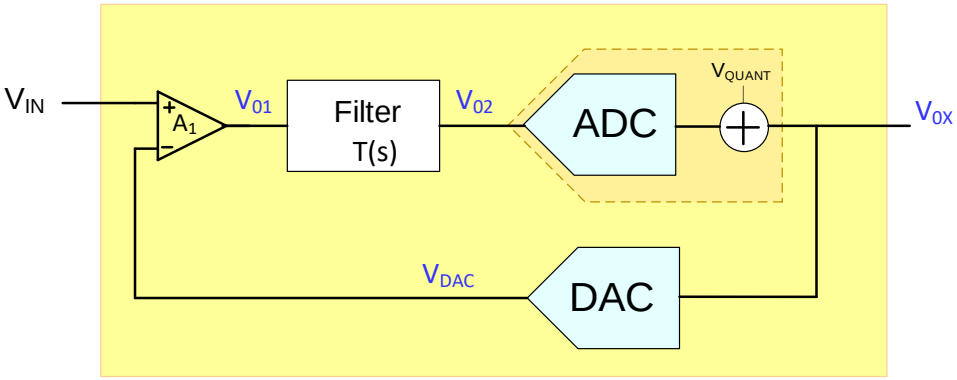




1. Increasing resolution of DAC, OSR, and filter order (in the right way) all offer potential for increasing ENOB
2. Output is not completely repeatable for a given input
3. Some dc inputs will introduce idle tones or spectral lines in the output
4. Dynamic range requirements for both the filter and the ADC may be high to avoid saturation
5. Stability analysis may be challenging and require extensive time-domain simulations (because of nonlinearities, analytically not practical)
6. OSDS-ADCs are insensitive to errors in ADC though ADC errors may increase the amount of over-range required for filter
7. Although nonlinearity in the signal-band of the filter is important, it is usually not difficult to obtain
8. Nonlinearity errors of the DAC directly introduce nonlinearity in the OSDS-ADC so excellent DAC linearity is generally required
9. Dead zones (input regions with no output) may exist

Higher-order Delta-Sigma ADC

(big benefit is noise shaping)



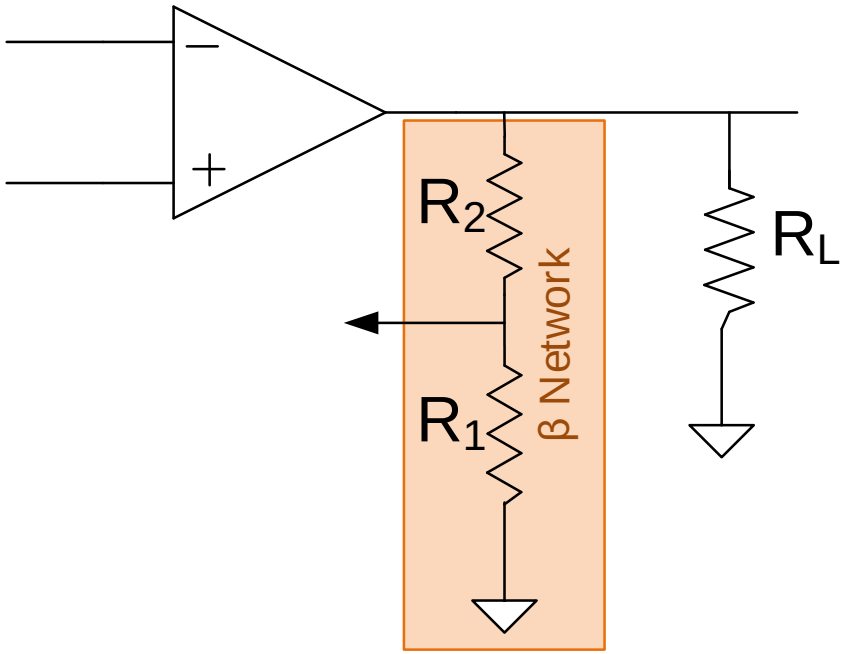
Excellent Material on Delta-Sigma ADCs

"How delta-sigma ADCs work (Part 1 and Part 2)"

Author: Bonnie Baker

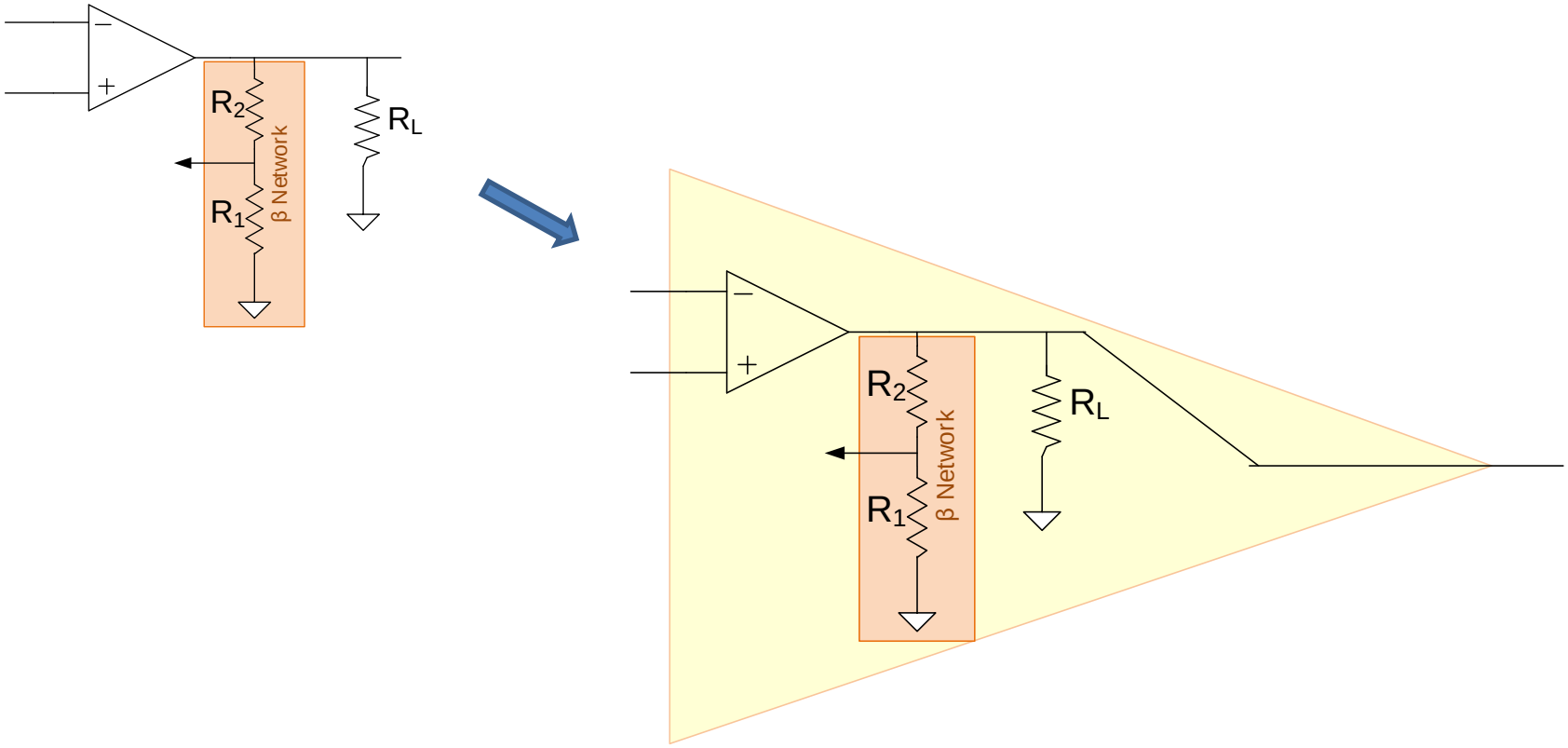
SLYT423 Revised Sept 2016 by Texas Instruments

Output Stages



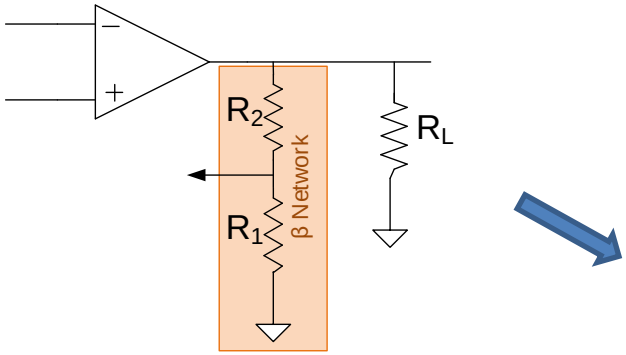
- Resistive Loading of Op Amp by R_L or β network reduces effective open loop gain
- Gain for most op amp architectures is increased by increasing output impedance
- Effective gain reduction can be dramatic

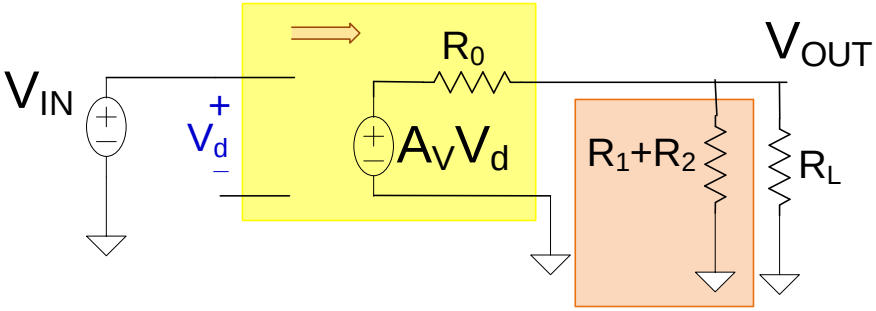
Output Stages



Approximate Equivalent Open-Loop Amp

Output Stages

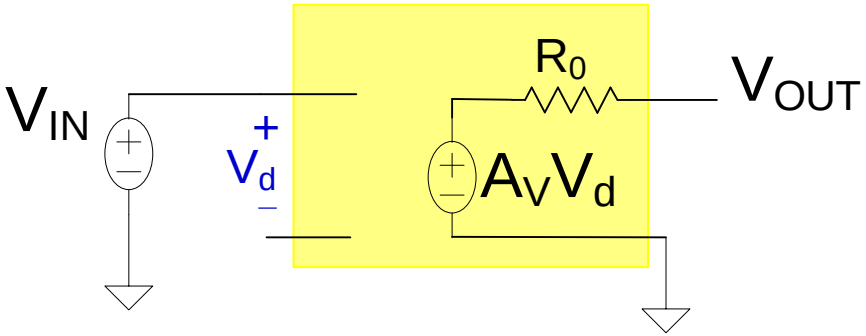




$$A_{VEFF} = A_V \frac{R_L \,//\, (R_1 + R_2)}{R_O + R_L \,//\, (R_1 + R_2)}$$

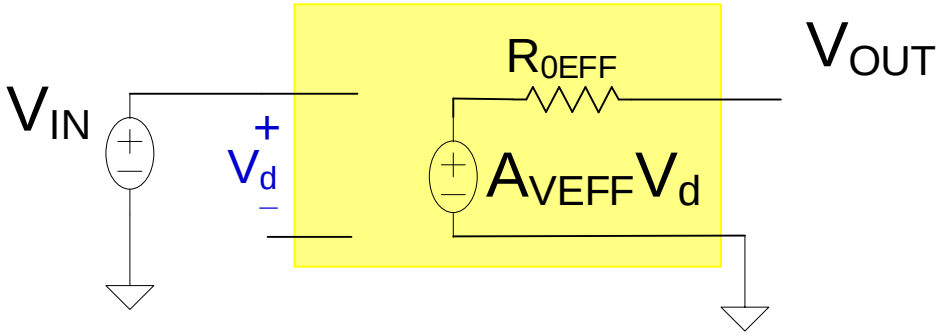
$$R_{OEFF} = R_O \,//\, R_L \,//\, (R_1 + R_2)$$

Output Stages



Approximate Equivalent Open-Loop Amp

Includes Resistive Loading of Load and β Network



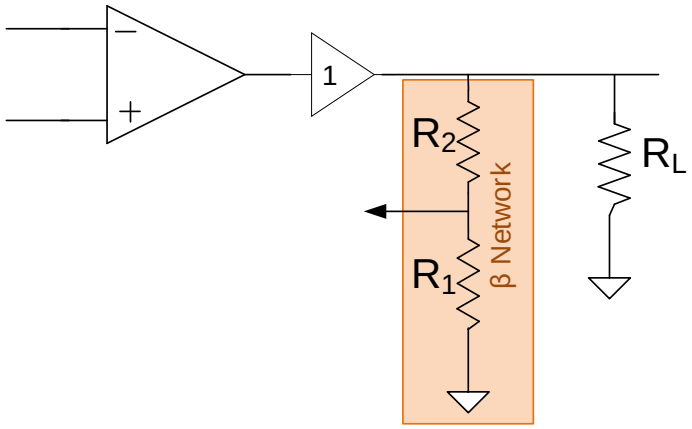
$$A_{VEFF} = A_V \frac{R_L \,//\, (R_1 + R_2)}{R_O + R_L \,//\, (R_1 + R_2)}$$

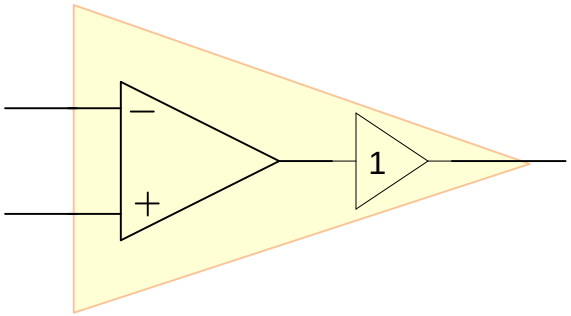
$$R_{OEFF} = R_O \,//\, R_L \,//\, (R_1 + R_2)$$

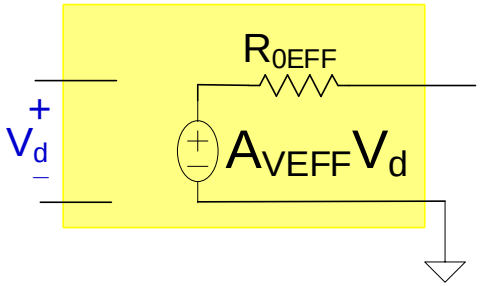
Output Stages

Conceptual Solution to Resistive Loading Problem:

Add Buffer between Op Amp and Resistive Load







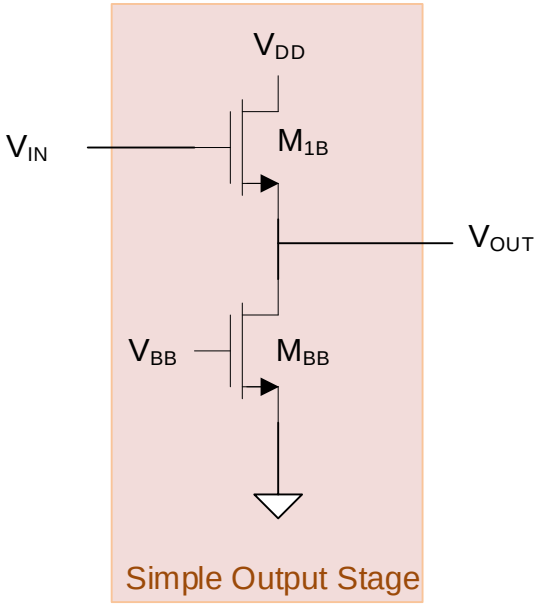
Approximate Equivalent Open-Loop Amp

$$A_{VEFF} = A_V$$

$$R_{OEFF} = R_{O-Buffer} \simeq 0\Omega$$

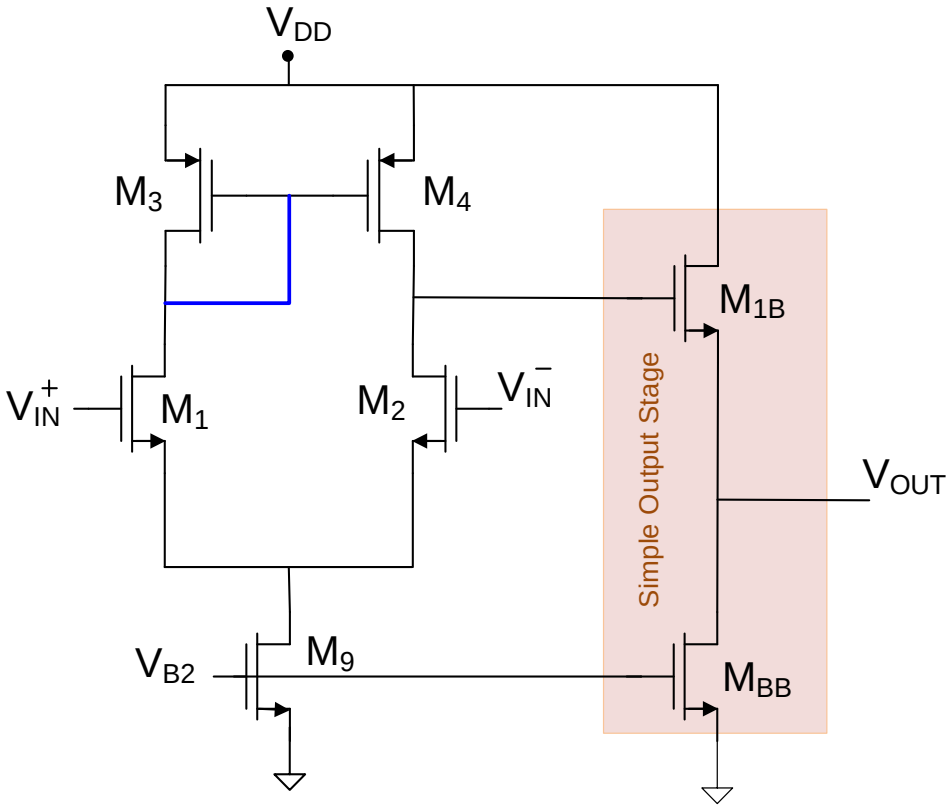
Buffer Termed Output Stage

Output Stages



- Recognized as Common Drain Amplifier
- Termed a Class A Amplifier
- Excellent Frequency Response
- Low Output Impedance and High Input Impedance
- Simple
- Output Signal Swing Reduced
- Power Dissipation in Class A Amplifiers Typically Considered Large

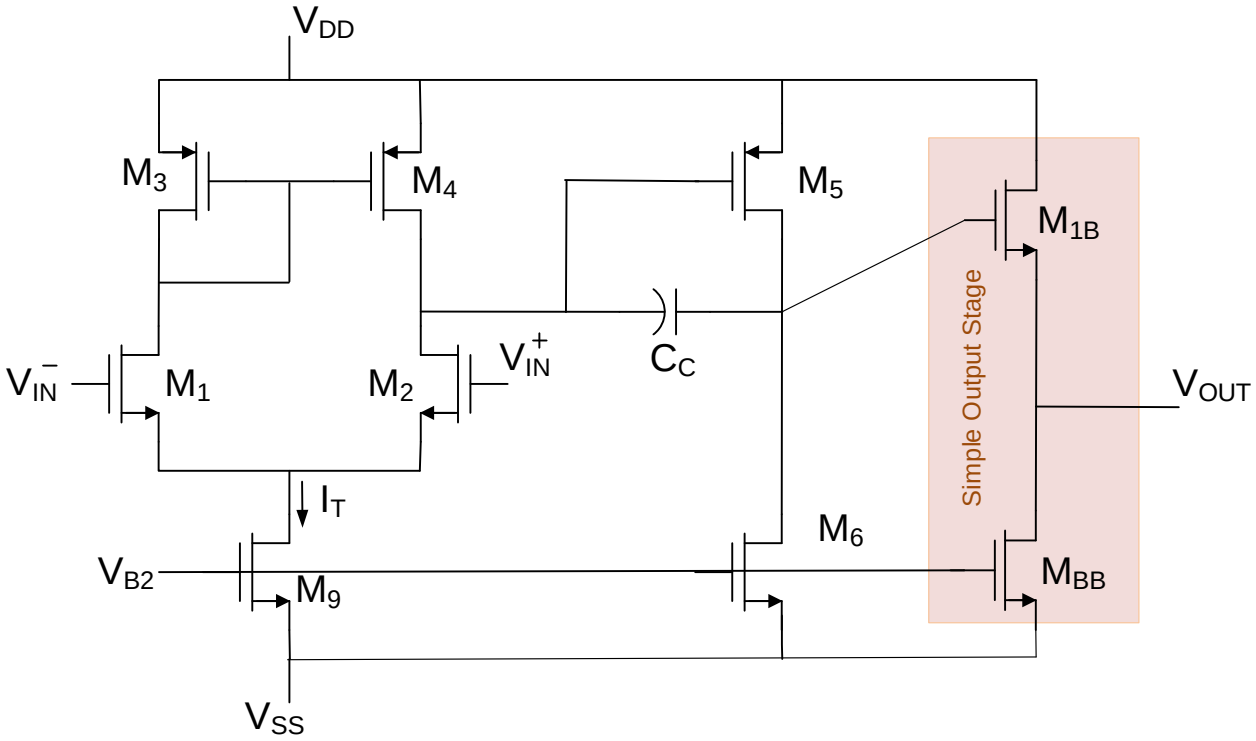
Output Stages



5T Op Amp with Output Stage

Technically 2-Stage but Pole of Output Stage at High Frequencies so often classified as Single-Stage

Output Stages

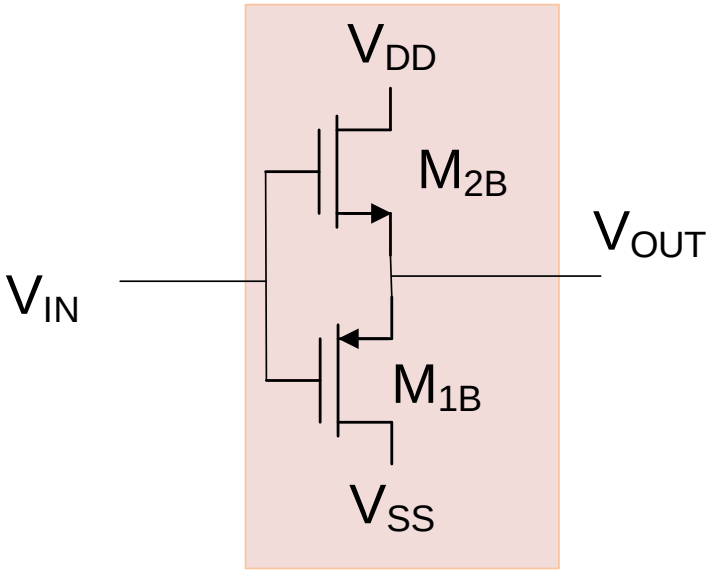


7T Op Amp with Output Stage

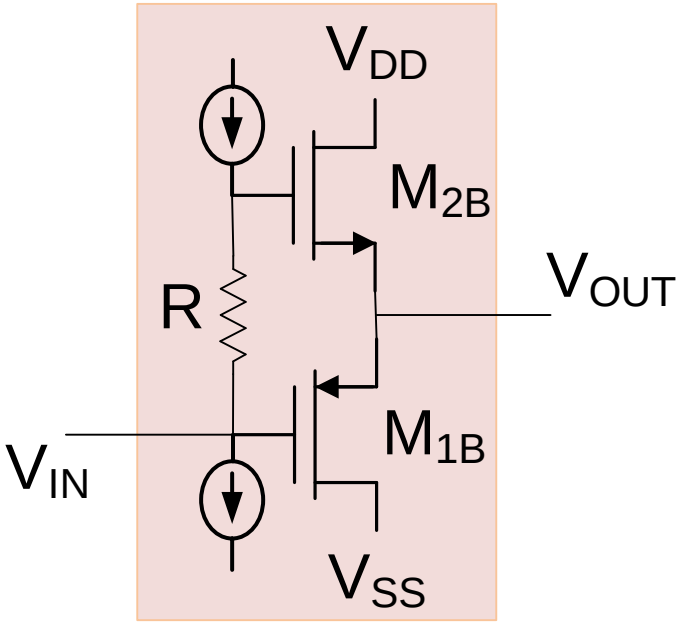
Technically 3-Stage but Pole of Output Stage at High Frequencies so often classified as two-stage

Note C_C often comes from output of second stage but could come from V_{OUT}

Other Output Stages

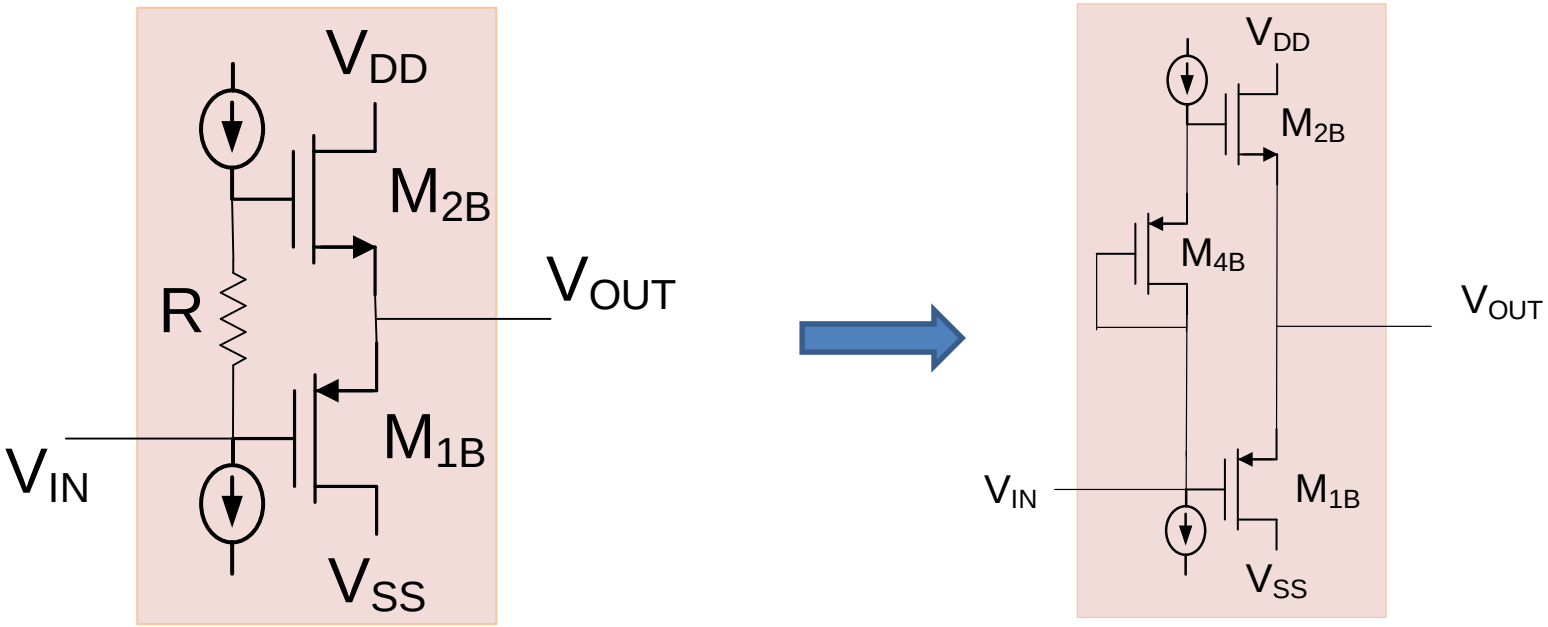


- Push-Pull
- Class B
- Cross-over Distortion
- More power efficient at Low Output Levels



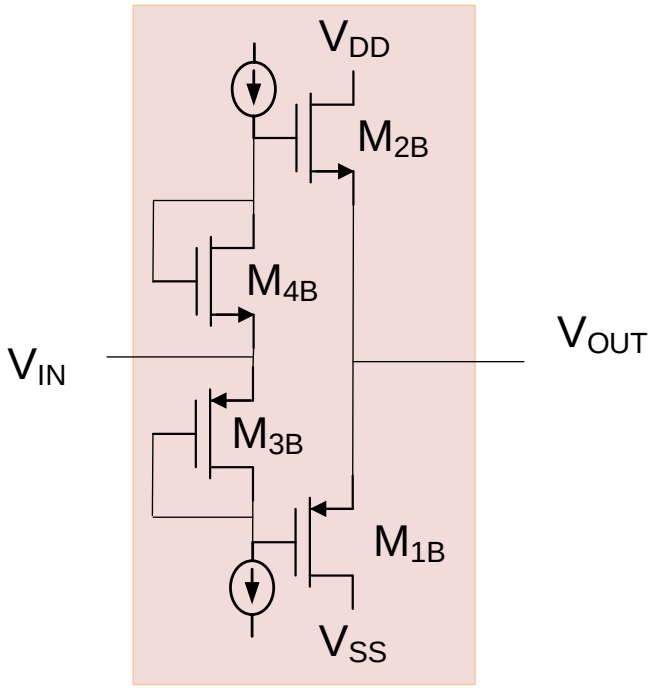
- Push-Pull
- Class AB
- Reduced Cross-over Distortion
- More power efficient at Low Output Levels than Class A

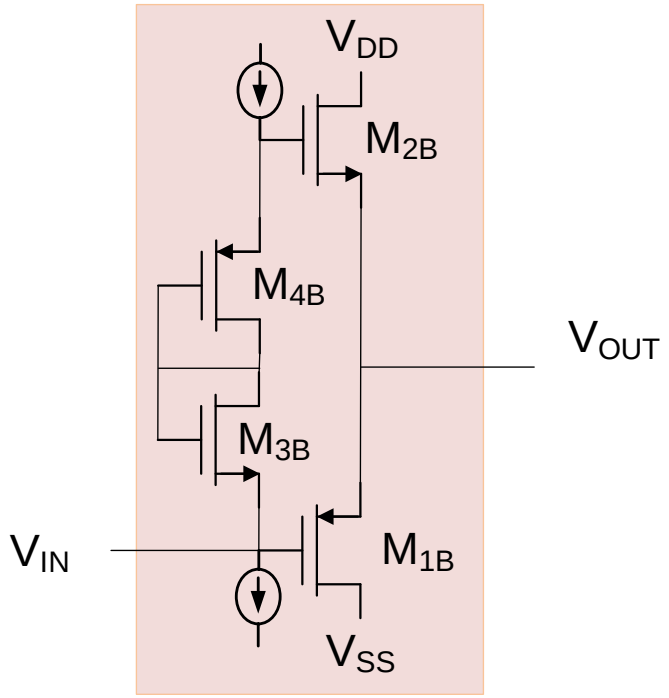
Other Output Stages



- Push-Pull
- Class AB
- Reduced Cross-over Distortion
- More power efficient at Low Output Levels than Class A

Other Output Stages





- Push-Pull
- Class AB
- Reduced Cross-over Distortion
- More power efficient at Low Output Levels than Class A

Stay Safe and Stay Healthy !

End of Lecture 42